In the Claims

Applicant has submitted a new complete claim set showing marked up claims with insertions indicated by underlining and deletions indicated by strikeouts and/or double bracketing.

Please cancel claims 1 and 31 without prejudice or disclaimer.

Please amend pending claims 2, 29, 30, 32, and 33 as noted below.

Listing of the Claims

1. (canceled)

2. (currently amended) ~~The~~ A communication circuit, comprising: ~~claimed in claim 1~~

an all-digital loop circuit configured to output a sample rate control signal to be a function of a frequency of a reference signal received by the communication circuit;

a variable-ratio sample rate filter that changes a sample rate of an output digital data stream relative to a sample rate of an input digital data stream in response to the sample rate control signal received from the all-digital loop circuit;

~~wherein the communication circuit further comprises~~ an analog-to-digital converter coupled to the variable-ratio sample rate filter; [[,]] and

a fixed clock coupled to the analog-to-digital converter to substantially fix a sampling rate of the analog-to-digital converter.

3. (previously presented) The communication circuit claimed in claim 2 wherein the variable-ratio sample rate filter comprises a digital decimation filter.

4-28 (canceled)

29. (currently amended) ~~The~~ A communication circuit, comprising: ~~claimed in claim 1~~

an all-digital loop circuit configured to output a sample rate control signal to be a function of a frequency of a reference signal received by the communication circuit; and

a variable-ratio sample rate filter that changes a sample rate of an output digital data stream relative to a sample rate of an input digital data stream in response to the sample rate control signal received from the all-digital loop circuit,

wherein the reference signal comprises a pilot tone signal.

30. (currently amended) ~~The~~ A communication circuit, comprising: ~~claimed in claim 1~~

an all-digital loop circuit configured to output a sample rate control signal to be a function of a frequency of a reference signal received by the communication circuit;

a variable-ratio sample rate filter that changes a sample rate of an output digital data stream relative to a sample rate of an input digital data stream in response to the sample rate control signal received from the all-digital loop circuit;

~~wherein the communication circuit further comprises~~ a digital-to-analog converter coupled to the variable-ratio sample rate filter; [[,]] and

a fixed clock coupled to the digital-to-analog converter to substantially fix a sampling rate of the digital-to-analog converter.

31. (canceled)

32. (currently amended) The communication circuit claimed in claim 30 ~~31~~ wherein the variable-ratio sample rate filter comprises an interpolation filter, and the interpolation filter comprises an ADSL interpolation filter.

33. (currently amended) The communication circuit claimed in claim 30 ~~31~~ wherein the variable-ratio sample rate filter comprises an interpolation filter, and the interpolation filter comprises a POTS interpolation filter.

34. (previously presented) The communication circuit claimed in claim 3 wherein the decimation filter comprises an ADSL decimation filter.

35. (previously presented) The communication circuit claimed in claim 3 wherein the decimation filter comprises a POTS decimation filter.

36. (previously presented) The communication circuit claimed in claim 2 wherein the communication circuit further comprises a second variable-ratio sample rate filter, and a digital-to-analog converter coupled to both the second variable-ratio sample rate filter and the fixed clock to substantially fix a sampling rate of the digital-to-analog converter.

37. (previously presented) The communication circuit claimed in claim 36 wherein the variable-ratio sample rate filter comprises a decimation filter, and the second variable-ratio sample rate filter comprises an interpolation filter.

38. (previously presented) The communication circuit claimed in claim 37 wherein the decimation filter comprises an ADSL decimation filter and the interpolation filter comprises an ADSL interpolation filter.

39. (previously presented) The communication circuit claimed in claim 37 wherein the decimation filter comprises a POTS decimation filter and the interpolation filter comprises a POTS interpolation filter.